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(54) Title: DEEP TRENCH ETCHING METHOD TO REDUCE/ELIMINATE FORMATION OF BLACK SILICON

(57) Abstract: In a method of etching a wafer to form a DT (deep trench) in a plasma reactor, wherein the wafer temperature is greater than the cathode temperature, the improvement of conducting etching to reduce or eliminate "black silicon", comprising:a) providing a plasma etch reactor comprising walls defining an etch chamber; b) providing a plasma source chamber remote from and in communication with the etch chamber, and a wafer chuck or pedestal disposed in the etch chamber to seat a wafer; c) forming a plasma within the plasma source chamber and providing the plasma to the etch chamber; d) supplying RF energy to etch the wafer to a point where the wafer temperature is greater than the cathode temperature; and e) increasing the flow rate of fluorine species near the end of the DT process to provide the isotropic component needed to widen the CD.

DEEP TRENCH ETCHING METHOD TO REDUCE/ELIMINATE FORMATION OF BLACK SILICON

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention generally relates to the reduction/elimination of black silicon during DT etch of a silicon wafer by manipulating the RF power, wafer temperature or fluorinate gaseous flow.

2. Description of Related Art

Integrated circuit (IC) technology has moved from large-scale integration (LSI) to very large scale integration (VLSI) and is soon expected to grow to ultra-large scale integration (ULSI). These advancements in monolithic circuit integration is due to improvements in manufacturing equipment and the materials and methods used in preparing semiconductor wafers into IC chips.

In this technology, several factors impose increasingly strict requirements on the basic integrated circuit fabrication steps of: masking; film formation; doping and etching; and dielectric insulation.

These factors are: the incorporation of IC chips into increasingly complex devices and circuits; the use of greater device densities and smaller feature sizes, and smaller separation; the use of composite conductor layers; and the use of the third wafer dimension of depth as well as the surface area to form buried or trench capacitors (DT).

In this connection, the ability to etch narrow, deep, high aspect ratio trenches is vital to the formation of buried or trenched capacitors. Further, single crystal silicon trench isolation is increasingly being used in semiconductor research as an alternative to other device isolation technologies, due to the fact that trench dielectric isolation offers a number of advantages, such

as relatively small surface area requirements, small width-to-depth ratios, and a vertical wall profile.

A further and significant advantage of the trench technology is its relative simplicity of process. For example, to create a buried capacitor or dielectric isolation structure using trench technology entails reactive ion etching (RIE) a groove into a single crystal silicon substrate, oxidizing side walls of the groove or trench, filling the groove with oxide dielectric or a polysilicon, and planarizing the surface.

However, "black silicon" is one of the prevalent etch obstacles during the etching process. Black silicon is caused by the presence of surface contaminates such as residual oxides, that act as localized etched mask. Consequently, the areas beneath these micromasks are not etched away until the contaminates are completely eroded, thereby causing the bottom of the finished trenched substrate to develop a rough, light-scattering dark surface appearance that is responsible for the name "black silicon".

Black silicon formation may also be formed at the edge of a wafer and can cause loss of chips and therefore directly contributes to chip yield loss.

One of the mechanisms for black silicon formation is the erosion of the boron doped silicate glass (BSG) mask at the edge that causes the exposure of the silicon surface. The higher BSG/Nitride etch rate at the periphery of the wafer is caused by the focusing of ions from the focusing dielectric ring placed around the wafer in the DT (deep trench) etch tool.

US Patent 5,874,362 disclose a method for etching a high aspect ratio, straight walled opening in silicon, in which the opening is characterized by a rounded bottom. The process is conducted by forming a plasma from a precursor gas etch mixture of HBr as the main etchant, using oxygen to provide protection for the side walls of the openings and to control selectivity with respect to the oxide etch mask, employing a fluorine-containing gas to remove residual contaminates from the side walls of the openings, and etching a silicon body until an opening of the desired depth is formed. The use of a brominate and gas chemistry in this process is said to overcome the problem of black silicon.

A method of and apparatus for improving etch uniformity in remote source plasma reactors with a powered wafer chuck or pedestal is disclosed in US Patent 5,662,770. The invention addresses the uniformity problem which arises due to non-uniform power coupling between a wafer and the walls of the etch chamber by increasing the impedance between the wafer and the chamber walls by placing a cylindrical dielectric quartz wall around the wafer if silicon is to be etched selectively with respect to silicon dioxide.

A plasma etch apparatus with heated scavenging surfaces is disclosed in US Patent 5,477,975. The plasma etch reactor is operated by introducing a gas into the reactor which disassociates as a plasma into an etched species which etches oxide films on a work piece in the reactor and a non-etching species combinable with the etched species into an etch-preventing polymer condensable onto the work piece below a certain deposition temperature, thereby providing an interior wall comprising a material which scavenges the etching species, and maintains a temperature of the interior wall above the deposition temperature.

US Patent 5,292,399 disclose a plasma etching apparatus with conductive means for inhibiting arcing. The conductive means for inhibiting arcing from electrical charges accumulating on one or more non-conductive protective surfaces on members at Rf potential within the apparatus includes one or more conductive plugs extending through one or more of the protective surfaces or a conductive ring surrounding the wafer on the top surface of a metal pedestal.

As the critical dimensions decrease, the open silicon area available for DT etch also reduces, culminating in the reduction of the average silicon etch rate. This results in lower corner selectivity (selectivity in the array) between the c-Si and the oxide mask. This problem is more severe on the edge since the chip on the edge has few nearest neighbors. This results in mask erosion and formation of black silicon.

SUMMARY OF THE INVENTION

One object of the present invention is to provide a process during DT etch in which the etch rate of the oxide is reduced after achieving a certain aspect ratio (trench depth) while maintaining a constant etch rate of silicon.

Another object of the present invention is to provide a process during deep trench etching or reduction/elimination of black silicon on the wafer by manipulating the RF power.

A further object of the present invention is to provide a process during DT etch for reduction/elimination of black silicon on the wafer by manipulating the wafer temperature.

A still further object of the present invention is to provide during a process of DT etch for reduction/elimination of black silicon on the wafer by manipulating the fluorinate gaseous flow.

In general, the invention is accomplished by maintaining the same deferential etch rate of silicon by reducing the applied RF power gradually after a certain trench depth is achieved, to sustain the deferential etch rate of silicon by providing the desired flux of neutral species, while reducing the oxide etch rate (by reducing the ion energy) to protect the silicon at the wafer edge from being exposed to plasma, thereby eliminating or minimizing the formation of black silicon.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT OF THE INVENTION

The invention constitutes a new method for deep trench etching to reduce/eliminate formation of black silicon, which is one of the prevalent etch obstacles during the etching process. Black silicon is caused by the presence of surface contaminates such as residual oxides, that act as localized etched mask.

In this connection, it has been observed that areas beneath the micromask are not etched away until the contaminates are completely eroded, thereby causing the bottom of the finished trenched substrate to develop a rough, light-scattering dark surface appearance that is responsible for the name "black silicon".

Still further, black silicon formation may also be formed at the edge of a wafer and may cause loss of chips and thereby contribute to chip yield loss.

It is known that one of the mechanisms for black silicon formation is the erosion of the boron doped silicate glass (BSG) mask at the edge that causes the exposure of the silicon surface. The higher BSG/nitride etch rate at the periphery of the wafer is caused by the focusing of ions from the focusing dielectric ring placed around the wafer in the DT (deep trench) etch tool.

The invention process employs a method whereby the etch rate of the oxide is reduced after achieving a certain aspect ratio (trench depth) while maintaining a constant etch rate of silicon.

In the invention process scheme, wafers are prepared with standard oxide mask stack. The deep trench mask is opened with the process of record (POR) in the POR tool.

In the invention process, the deep trench etch conditions can be such that the wafer temperature is less than the cathode temperature or vice versa. During etching, the etch rate of the oxide mask remains constant, being that it is the top horizontal plane, and undergoes no RIE lag. On the other hand, the silicon surface is being recessed at a much higher rate. The ion/neutral transport to the bottom of the trench becomes critical at larger trench depths.

Furthermore, ions often undergo collisions with the sidewall passivation film, thereby loosing energy and thereby reducing the silicon etch rate. Accordingly, the dynamics is such that, as the aspect ratio increases with time, the differential etch rate of silicon decreases while the oxide etch rate remains unchanged.

The etch rate of oxide mask is a strong function of applied RF power since ion bombardment is required to break the Si-O bonds. Increasing the RF power, on the other hand, does not contribute towards higher silicon etch rate, which is being limited by the neutral flux at the trench bottom. However, the high power can expose the silicon due to loss of the mask at the edge of the wafer, and the exposed silicon causes black silicon.

In the invention process, there is maintenance of the same differential etch rate of silicon even when gradually reducing the applied RF power after a certain trench depth is achieved.

Accordingly, in the invention process, there is a sustaining of the differential etch rate of silicon by providing the desired flux of neutral species, while reducing the oxide etch rate (by reducing the ion energy). This approach keeps the silicon wafer edge protected from being exposed to plasma, thereby eliminating /minimizing the formation of black silicon.

EXAMPLE 1

In the method of etching a wafer to form a DT wherein the wafer temperature is greater than the cathode temperature, reduction of the "black silicon" is obtained by: providing a plasma etch reactor comprising walls defining an etch chamber; providing a plasma source chamber remote from and in communication with the etch chamber, and a wafer chuck or pedestal disposed in the etch chamber to seat a wafer; forming a plasma within the plasma source chamber and providing the plasma to the etch chamber; supplying RF energy to etch the wafer to a point where the wafer temperature is greater than the cathode temperature; and increasing the flow rate of fluorine species near the end of the DT process to provide the isotropic component needed to widen the CD.

EXAMPLE 2

In the process of etching a wafer to form a DT wherein the wafer temperature is greater than the cathode temperature, an alternative approach to eliminating "black silicon" is accomplished by: providing a plasma etch reactor comprising walls defining an etch chamber; providing a plasma source chamber remote from and in communication with the etch chamber, and a wafer chuck or pedestal disposed in the etch chamber to seat a wafer; forming a plasma within the plasma source chamber and providing the plasma to the etch chamber; supplying RF energy to etch the wafer to a point where the wafer temperature is greater than the cathode temperature; and decreasing the RF power to reduce the wafer temperature to provide profiles with a narrower bottom CD.

EXAMPLE 3

When preparing a DT by etching a wafer in which the cathode temperature is higher than the wafer temperature, reduction of the "black silicon" is accomplished by: providing a plasma etch reactor comprising walls defining an etch chamber; providing a plasma source chamber remote from and in communication with the etch chamber, and a wafer chuck or pedestal disposed in the etch chamber to seat a wafer; forming a plasma within the plasma source chamber and providing a plasma to the etch chamber; supplying RF energy to etch the wafer to a point where the cathode temperature is higher than the wafer temperature; and increasing the cathode temperature to maintain the wafer temperature.

In the context of the invention, the fluorine species to etch the wafer may be selected from SiF_4, SF_6 and NF_3.

When the cathode temperature is higher than the wafer temperature during preparation of the DT, elimination of black silicon is accomplished by increasing the flow rate of a fluorine species to compensate for loss of CD caused by the reduced wafer temperature and increasing the cathode temperature up to about 300°C to maintain the existing lower wafer temperature.

We claim:

1. In a method of etching a wafer to form a DT (deep trench) in a plasma reactor, wherein the wafer temperature is greater than the cathode temperature, the improvement of conducting etching to reduce or eliminate "black silicon", comprising:

a) providing a plasma etch reactor comprising walls defining an etch chamber;

b) providing a plasma source chamber remote from and in communication with said etch chamber, and a wafer chuck or pedestal disposed in said etch chamber to seat a wafer;

c) forming a plasma within said plasma source chamber and providing said plasma to said etch chamber;

d) supplying RF energy to etch said wafer to a point where the wafer temperature is greater than the cathode temperature; and

e) increasing the flow rate of fluorine species near the end of the DT process to provide the isotropic component needed to widen the CD.

2. In a method of etching a wafer to form a DT (deep trench) in a plasma reactor, wherein the wafer temperature is greater than the cathode temperature, the improvement of conducting etching to reduce or eliminate "black silicon", comprising:

a) providing a plasma etch reactor comprising walls defining an etch chamber;

b) providing a plasma source chamber remote from and in communication with said etch chamber, and a wafer chuck or pedestal disposed in said etch chamber to seat a wafer;

c) forming a plasma within said plasma source chamber and providing said plasma to said etch chamber;

d) supplying RF energy to etch said wafer to a point where the wafer temperature is greater than the cathode temperature; and

e) decreasing the RF power to reduce the wafer temperature to provide profiles with a narrower bottom CD.

3. In a method of etching a wafer to form a DT (deep trench) in a plasma reactor, wherein the wafer cathode temperature is higher than the wafer temperature and creates loss of CD at a given RF power, the improvement of conducting etching to reduce or eliminate "black silicon", comprising:

a) providing a plasma etch reactor comprising walls defining an etch chamber;

b) providing a plasma source chamber remote from and in communication with said etch chamber, and a wafer chuck or pedestal disposed in said etch chamber to seat a wafer;

c) forming a plasma within said plasma source chamber and providing a plasma to said etch chamber;

d) supplying RF energy to etch said wafer to a point where the cathode temperature is higher than the wafer temperature; and increasing the flow rate of a fluorine species to compensate for loss of CD caused by the reduced wafer temperature and increasing said cathode temperature to maintain said wafer temperature.

4. The process of claim 3 wherein in step e) said cathode temperature is increased to about 300°C.

5. The process of claim 1 wherein the fluorine species is selected from the group consisting of SiF_4, SF_6 and NF_3.

6. The process of claim 2 wherein the fluorine species is selected from the group consisting of SiF_4, SF_6 and NF_3.

7. The process of claim 3 wherein the fluorine species is selected from the group consisting of SiF_4, SF_6 and NF_3.

8. The process of claim 4 wherein the fluorine species is selected from the group consisting of SiF_4, SF_6 and NF_3.

9. The process of claim 5 wherein the fluorine species is SF_6.

10. The process of claim 6 wherein the fluorine species is SF_6.

11. The process of claim 7 wherein the fluorine species is SF_6.

12. The process of claim 8 wherein the fluorine species is SF_6.